3.5 Carbon Nanotube Transistor Circuits: Circuit-Level Performance Benchmarking and Design Options for Living with Imperfections

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Carbon Nanotubes Field Effect Transistors (CNFETs) are promising candidates as extensions to Si CMOS due to excellent CV/I device performance [1]. The objective of this work is to analyze speed and power of CNFET circuits and their tolerance to imperfections inherent to CNFET synthesis such as misaligned and metallic Carbon Nanotubes (CNTs) and CNT diameter and doping variations. Also demonstrated are design principles for CNFET-based logic circuits that are guaranteed to implement correct logic functions even in the presence of misaligned CNTs. The motivation of this research is: given the opportunities with CNFET devices – fine pitch, excellent CNFET device characteristics –what can be gained at the circuit-level compared to cutting-edge Si CMOS?

The circuit simulations in this paper use a CNFET HSPICE model that includes practical device non-idealities [2, 3]. A 0.9V power supply is used for both CNFET and CMOS circuits [4]. Single CNFET devices are 13× and 6× faster than pMOS and nMOS with a similar gate length based on the intrinsic CV/I gate delay metric. While similar numbers are often quoted in the literature [5], these numbers are optimistic because local interconnect capacitances and CNT imperfections are not considered.

Figure 3.5.1 shows the layout of a CNFET inverter with multiple CNTs. Gates and contacts are defined by lithography. A five-stage FO4 inverter chain is simulated consisting of CNFETs with no imperfections (CNT diameter = 1.5nm, Doping = 1%). The CNFET inverters are minimum sized with 32nm gate width. The first simulation setup consists of inverters with single semiconducting CNTs. The 3rd CNFET inverter stage in the chain is ~2× faster and has ~6× lower switching energy per cycle compared to a 32nm Si CMOS inverter using a similar setup (modeled using the BSIM predictive model [6]). Note that the delay advantage is smaller than the intrinsic CV/I delay advantage reported above. This is because, unlike in CMOS circuits, the local interconnect capacitance dominates the gate capacitance in CNFET circuits (Fig. 3.5.2, Fig. 3.5.7). Next, the delay through the 3rd stage is measured while increasing the number of CNTs per inverter for all inverters without changing their gate widths. The FO4 delay through the 3rd stage initially improves because of increased drive current (Fig. 3.5.3). The delay subsequently worsens due to reduced gate-to-CNT capacitance as a result of increased inter-CNT charge screening. A 4nm minimum CNT pitch (8 tubes per 32nm of gate width) gives optimal delay (Fig. 3.5.3).

The previous analysis assumed perfect CNTs. In reality, there are limitations with CNT manufacturing technology over and above process variations introduced by lithography. These are: 1) Doping variations in CNFET source and drain regions that cause drive current variations [7]; 2) CNT diameter variations that cause variations in the CNFET drive current [2, 8]; 3) Metallic CNTs that cannot be used to make CNFETs. A metallic CNT causes a short between the source and the drain of a CNFET. For a random distribution of CNT chirality, about 1/3 of the CNTs are metallic [9]. Current CNT synthesis techniques yield between 10% to 70% metallic CNTs [10]. One can, in principle, attain the target current drive in a CNFET inverter by starting with a larger number of CNTs (mixture of semiconducting and metallic) and then removing the metallic CNTs (e.g. by electrical burning [11] or chemical etching [12]). In this paper, we assume that all metallic CNTs can be removed by a perfect removal process. Even in this optimistic scenario, the number of remaining semiconducting CNTs per inverter becomes stochastic variables, causing significant drive current variations; 4) Misaligned CNTs that can cause unintended shorts inside logic structures as shown for the static NAND structure in Fig. 3.5.5. The best CNT synthesis techniques today produce misaligned CNTs like the ones shown in the SEM photo of Fig. 3.5.5 [13].

To quantify the effects of CNFET doping variations, CNT diameter variations, and variations caused by removal of metallic CNTs, the following separate Monte-Carlo simulations were performed. The same inverter chain described before is used assuming perfectly aligned and uniformly spaced tubes with a minimum pitch of 4nm. The following parameters of the test inverter (the 3rd stage in the inverter chain) are individually varied (Fig. 3.5.7): 1) Source / drain doping levels; 2) CNT diameters; 3) Probability of a CNT to be metallic.

Compared is the mean, 3σ, and 6σ values of the FO4 delay and energy per cycle of this test inverter to those of a 32nm Si CMOS test inverter in a CMOS inverter chain (without any process variations). The impact of CNFET doping variations and CNT diameter variations on delay and energy per cycle is not significant compared to the impact of variations caused by 32% metallic CNTs (Fig. 3.5.6, Fig. 3.5.4). For devices targeted to have 4 or fewer CNTs, there is a non-negligible probability that all CNTs in the device are metallic and therefore removed, causing an open circuit. Thus the probability of metallic CNTs sets a lower bound on the minimum number of CNTs required per logic gate in order to make viable circuits. The speed and energy per cycle advantage improve if the probability of metallic CNTs before removal can be reduced to 8% (Fig. 3.5.6).

To address the problem of misaligned CNTs, a technique is described to design CNFET-based logic structures that are guaranteed to implement correct logic functions even in the presence of a large number of misaligned CNTs. Figure 3.5.5 illustrates this concept. Unlike the misaligned-CNT-vulnerable NAND gate, no CNT between V_{dd} and Output in the misaligned-CNT-immune-NAND is completely doped. This is because the gate regions can be lithographically masked during doping (Fig. 3.5.5). The misaligned-CNT-immune-NAND structure is ~25% larger in area compared to the misaligned-CNT-vulnerable-NAND structure. Misalignment statistics from CNT SEM images, such as those shown in Fig. 3.5.5, are currently being extracted to quantify the delay and energy per cycle impact of misaligned CNTs and misaligned CNT immune cell design.

In conclusion, much is to be gained from CNFET-based circuits (2.5× energy per cycle advantage and 4.6× FO4 delay advantage after addressing diameter and doping variations) over 32nm Si CMOS as long as circuits and architectures immune to misaligned CNTs and metallic CNTs can be built. As described in this paper, it is possible to design robust standard cells with guaranteed correct functionality in the presence of misaligned CNTs (Fig. 3.5.5). An interdisciplinary approach to overcome the problem of metallic CNTs is required. CNT synthesis techniques that can significantly and reliably reduce the probability of metallic CNTs (e.g., to fewer than 8% metallic CNTs) are extremely important. Novel CNT synthesis techniques need to be combined with reliable ways of removing metallic CNTs after CNT growth, together with new circuit and architectural techniques to fully overcome the challenge of metallic CNTs.

Acknowledgments:
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References:
[1] H.-S. P. Wong, et al., "Carbon Nanotube Field Effect Transistors – Fabrication, Device Physics, and Circuit Implications," *ISSCC Dig. Tech. Papers*, pp. 370 – 371, Feb., 2003.
[2] J. Deng, and H.-S. P. Wong, "A Circuit-Compatible SPICE model for Enhancement Mode Carbon Nanotube Field Effect Transistors," *Proc. Intl. Conf. Simulation of Semiconductor Processes and Devices,* pp. 166 – 169, Sept., 2006.
[3] I. Amlani, et al., "First Demonstration of AC Gain From a Single-walled Carbon Nanotube Common-Source Amplifier," *Proc. Intl. Electron Devices Meeting,* Paper 20.7, Dec., 2006.
[4] http://www.itrs.net/Links/2005ITRS/Home2005.htm
[5] J. Guo, et al., "Performance Analysis and Design Optimization of Near Ballistic Carbon Nanotube Field-Effect Transistors," *Proc. Intl. Electron Devices Meeting,* pp. 703 – 706, Dec., 2004.
[6] http://www.eas.asu.edu/~ptm/latest.html
[7] D. Kang, et al., "Oxygen-Induced P-type Doping of A Long Individual Single-walled Carbon Nanotube," *Nanotechnology*, vol. 16, pp. 1048 – 1052, 2005.
[8] Y-C Tseng, et al., "Effect of Diameter Variation in a Large Set of Carbon Nanotube Transistors," *Nano Letters,* vol. 6, pp. 1364 – 1368, 2006.
[9] R. Saito, G. Dresselhaus and M. Dresselhaus, "Physical Properties of Carbon Nanotubes," *Imperial College Press.*, London, UK, 1998.
[10] Y. Li, et al., "Preferential Growth of Semiconducting Single-Walled Carbon Nanotubes by a Plasma Enhanced CVD Method," *Nano Letters*, vol. 4, pp. 317, 2004.
[11] P. G. Collins, M. S. Arnold, and P. Avouris, "Engineering Carbon Nanotubes and Nanotube Circuits using Electrical Breakdown," *Science*, vol. 292, pp. 706 – 709, 2001.
[12] A. Hassanien, et al., "Selective Etching of Metallic Single-Wall Carbon Nanotubes with Hydrogen Plasma," *Nanotechnology*, vol. 16, pp. 278 – 281, 2005.
[13] S. Han, X. Liu, and C. Zhou, "Template-Free Directional Growth of Single-Walled Carbon Nanotubes on a- and r-Plane Sapphire," *J. Am. Chem. Soc.*, vol. 127, pp. 5294 – 5295, 2005.

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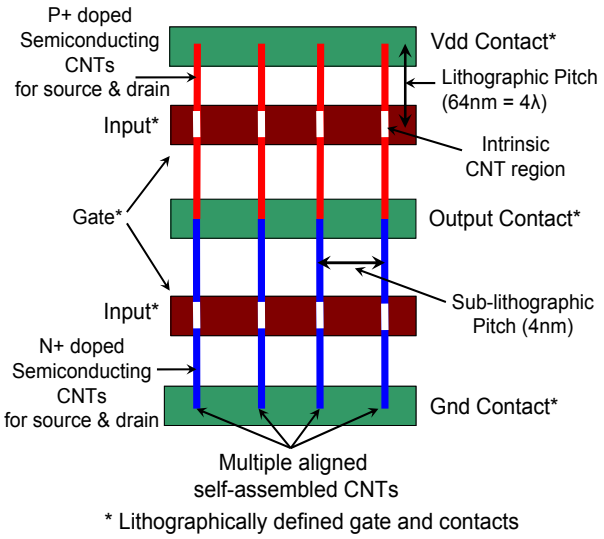
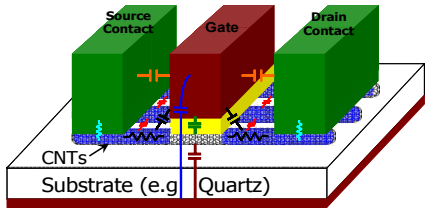


Figure 3.5.1: The layout of CNFET inverter with multiple CNTs per FET.



	Description	CNFET	MOSFET
C_{gc}	Gate to channel	~ 3 aF/CNT	1200 aF/μm
C_{gb}	Gate to Substrate	30 aF/μm gate width	N/A
C_{cb}	Tube to Substrate	20 aF/μm tube length	N/A
C_{cc}	Tube to Tube (Diff. Mode)	110 aF/μm tube length	N/A
C_{gs},C_{gd}	Gate to S/D Contact	78 aF/μm gate width *	600 aF/μm+
C_{gse},C_{gde}	Gate to S/D ext. Region	~ 0.5 aF/CNT *	
R_c	Contact Resistance	6.4 kΩ/Sub-band	40 Ω·μm

* The height of CNFET Gate/Source/Drain contacts: 64nm
+ Including junction capacitance

Figure 3.5.2: 3D view of a CNFET and associated capacitances and resistances.

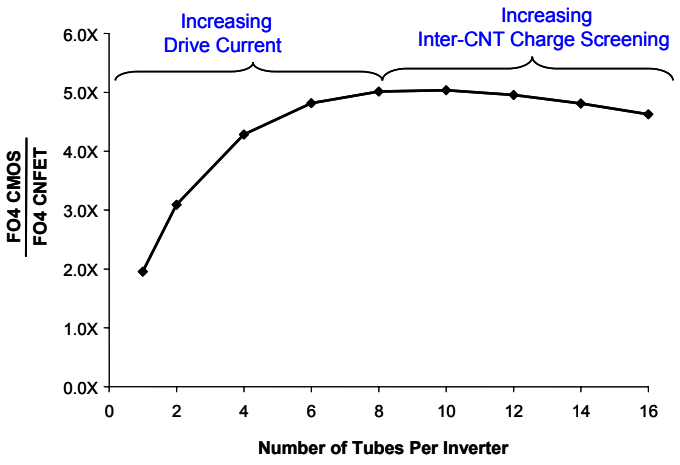


Figure 3.5.3: Mean FO4 delay improvement for CNFET inverter with no imperfections and a constant minimum size gate (varying CNT pitch) compared to 32nm Si CMOS.

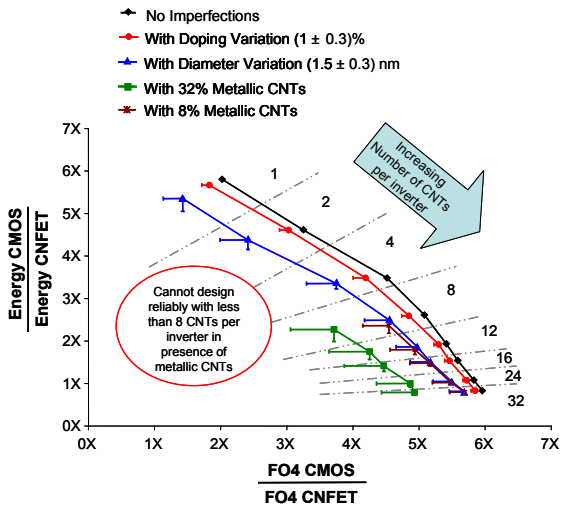


Figure 3.5.4: Energy per cycle and FO4 delay improvement for CNFET inverter at 3σ points (Minimum CNT pitch = 4nm and Minimum gate width = 32nm) compared to 32nm CMOS FO4 inverter (Error bars indicate 6σ variation).

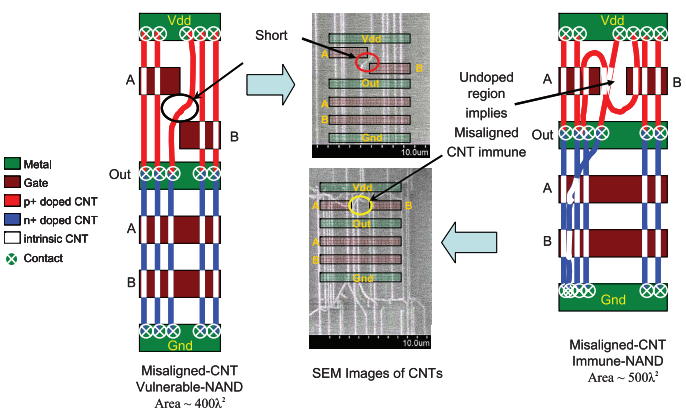


Figure 3.5.5: Misaligned-CNT vulnerable NAND cell (left) and misaligned-CNT immune NAND cell (right).

	Sources of CNFET Imperfections				
	No Imperfection	Doping Variation (1 ± 0.3)%	Diameter Variation (1.5 ± 0.3) nm	8% Metallic CNTs	32% Metallic CNTs
Mean FO4 delay (ps)	**2.95 ps**	**3.03 ps**	**3.00 ps**	**3.00 ps**	**3.17 ps**
Std. Dev. of FO4 delay (ps) [% mean]	–	**0.02 ps [0.5%]**	**0.09 ps [3.3%]**	**0.10 ps [3.5%]**	**0.29 ps [9.2%]**
FO4 delay advantage vs. 32 nm Si CMOS	**5.1×**	**5.0×**	**5.0×**	**5.0×**	**4.7×**
FO4 delay advantage vs. 32 nm Si CMOS (3σ delay)	–	**4.9×**	**4.6×**	**4.5×**	**3.7×**
FO4 delay advantage vs. 32 nm Si CMOS (6σ delay)	–	**4.7×**	**4.2×**	**4.2×**	**3.0×**
Energy per cycle advantage vs. 32 nm Si CMOS	**2.6×**	**2.6×**	**2.6×**	**2.6×**	**2.6×**
Energy per cycle advantage vs. 32 nm Si CMOS (3σ energy)	–	**2.6×**	**2.5×**	**2.4×**	**2.3×**
Energy per cycle advantage vs. 32 nm Si CMOS (6σ energy)	–	**2.6×**	**2.4×**	**2.2×**	**2.0×**

Figure 3.5.6: FO4 delay and energy per cycle gain for 8 CNTs per inverter in the presence of imperfections.

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Variable Parameters	
Source/Drain Doping Level	0.59eV - 0.75eV (0.7% - 1.3%) Uniformly distributed*
CNT Diameter	1.2nm - 1.8nm Uniformly distributed*
Probability of a CNT to be Metallic	8% - 32%
Fixed Parameters	
Oxide Thickness (T_{ox})	4nm
Gate Dielectric (Dielectric Constant:K_{ox})	HfO_2 (16)
CNT Pitch	4nm
Power Supply	0.9V
Mean Free Path: Intrinsic CNT	200nm
Mean Free Path: Doped CNT	15nm
Gate/Source/Drain Length (CNT)	32nm
Work Function: contact (Φ_M)	4.5eV
Work Function: CNT (Φ_{CNT})	4.5eV
Interconnect Capacitance	0.22fF/μm

* In the absence of large scale statistical data.

Figure 3.5.7: Device parameters and process assumptions for simulations.

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